REMARKS

Claims 1-27 are pending in the present application. Claims 1, 10 and 19 have been amended.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on May 25, 2001.

Information Disclosure Statement

An Information Disclosure Statement has been filed concurrently herewith. An English translation of the Japanese Patent Publication will promptly follow in due course, to supplement this submission. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement and the corresponding English translation thereof, and to confirm that the corresponding reference has been considered and will be cited of record in the present application.**

Claim Rejections-35 U.S.C. 102

Claims 1 and 8 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Nishiguchi reference (U.S. Patent No. 5,188,984). This rejection is respectfully traversed for the following reasons.

The method for manufacturing a semiconductor device of claim 1 includes in combination "forming a first insulating layer on a semiconductor substrate"; "forming a semiconductor layer on said first insulating layer"; "forming an insulating region on said first insulating layer to insulate said semiconductor layer"; "forming a conductive layer on said semiconductor layer after forming said insulating region"; and "implanting ions in said semiconductor layer after forming said conductive layer, thereby forming an active region within said semiconductor layer". Applicant respectfully submits that the Nishiguchi reference as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted substrate 51 in Figs. 2a – 2e of the Nishiguchi reference as the semiconductor substrate of claim 1, gallium arsenide chip 55 as the active region of claim 1, insulating film 56 as the insulating region of claim 1, and thin film connecting circuit pattern 57 as the conductive layer of claim 1. Applicant respectfully submits that the Examiner's interpretation of the Nishiguchi reference as meeting the above noted features of claim 1 is improper for at least the following reasons.

Particularly, the Nishiguchi reference does not form a conductive layer on a semiconductor layer, and thereafter implant ions in the semiconductor layer to thereby

form an active region within the semiconductor layer.

As described beginning in column 4, line 4 of the Nishiguchi reference, gallium arsenide chip 55 as a previously made device having an integrated circuit pattern with electrodes, is disposed in concave portion 54 of substrate 51. Gallium arsenide chip 55 is not an active region, but is more precisely a semiconductor chip. Moreover, gallium arsenide chip 55 is mounted on substrate 51 in an intermediate process step as shown in Fig. 2c of the Nishiguchi reference, **prior to** formation of thin film connecting circuit pattern 57 (interpreted by the Examiner as the conductive layer of claim 1) as shown in Fig. 2e. Accordingly, it should be readily clear that gallium arsenide chip 55 of the Nishiguchi reference is not an active region formed in a semiconductor layer by implanting ions after formation of a conductive layer, as would be necessary to meet the features of claim 1. Applicant therefore respectfully submits that the method for manufacturing a semiconductor device of claim 1 distinguishes over the Nishiguchi reference as relied upon by the Examiner, and that this rejection of claims 1 and 8 is improper for at least these reasons.

With further regard to this rejection, Applicant respectfully submits that the Nishiguchi reference does not implant ions into a semiconductor layer, and thus does not resultantly form an active region in a semiconductor layer, as asserted by the Examiner. The Examiner has noted that thin film connecting circuit pattern 57 as shown in Fig. 2e of the Nishiguchi reference is formed by sputtering of aluminum, and has asserted that this reads on the ion implanting of claim 1. However, as described in

column 4, lines 29-36 of the Nishiguchi reference, a thin film conducting layer is formed on the whole surface of insulating film 56 by sputtering aluminum, and the sputtered aluminum film is subsequently patterned to form upper thin film connecting circuit layer 57. Thus, the aluminum film is merely sputtered on insulating film 56. Clearly, sputtering in general cannot be interpreted as ion implantation. More particularly, this sputtering cannot be interpreted as ion implantation into a semiconductor layer to form an active region in the semiconductor layer as would be necessary to meet the features of claim 1, because sputtering in this case merely deposits aluminum on insulating film 56. Applicant therefore respectfully submits that the method for manufacturing a semiconductor device of claim 1 distinguishes over the Nishiguchi reference as relied upon by the Examiner, and that this rejection of claims 1 and 8 is improper for at least these additional reasons.

With further regard to this rejection, the Nishiguchi reference does not disclose forming a first insulating layer on a semiconductor substrate, and forming a semiconductor layer on the first insulating layer, as would be necessary to meet the further features of claim 1. That is, in the Nishiguchi reference, gallium arsenide chip 55 is merely disposed within concave portion 54 of substrate 51. Applicant therefore respectfully submits that the method for manufacturing a semiconductor device of claim 1 distinguishes over the Nishiguchi reference as relied upon by the Examiner, and that this rejection of claims 1 and 8 is improper for at least these additional reasons.

Claim Rejections-35 U.S.C. 103

Claim 2 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishiguchi reference in view of the Shimada reference (U.S. Patent No. 6,002,383). Claims 3-5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishiguchi reference in view of the Shimada reference, in further view of the Tsutsumi reference (U.S. Patent No. 5,789,792). Also, claims 6, 7 and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Nishiguchi reference in view of the Hara et al. reference (U.S. Patent No. 5,946,167). Applicant respectfully submits that the secondary references as relied upon by the Examiner do not overcome the above noted deficiencies of the primarily relied upon Nishiguchi reference. Accordingly, Applicant respectfully submits that the above noted claims distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 10-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant however respectfully notes that claims 10-27 should be allowable at least by virtue of dependency upon claim 1, and that further amendment of these claims to be in independent form is thus unnecessary.

Conclusion

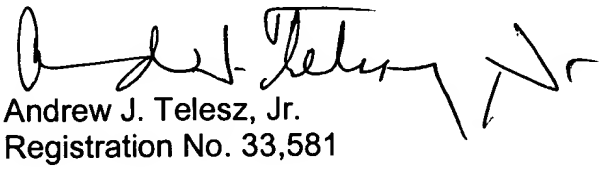
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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